STABILISING AMPLIFIER AM18/520

Introduction

This unit forms part of a Sync Pulse Stabilising Amplifier[1] and combines the functions of an AM1/570 Video Amplifier and an AM18/507 Processing Amplifier.

The video amplifier section of the unit accepts a coded colour-video signal and a colour-burst error signal[2]; it provides a video output signal in which the phase and amplitude of the colour-burst component of the video signal have been corrected by the addition of the burst-error signal. An auxiliary output, consisting of the uncorrected video input signal, is provided also.

The processing amplifier section accepts a composite video signal (the output of the video amplifier section after it has passed through a Video Source Switch Unit[3]) clamps it at blanking level, in conjunction with an Error Signal Amplifier[4], and removes by clipping any excessive amplitude of the luminance signal. The original sync pulses are removed from the signal by gating action and replaced by sync pulses of the correct shape and amplitude. The output consists of a composite video signal of standard amplitude.

The AM18/520 is mounted on a CH1/43 chassis with index-peg positions 3, 4 and 5. *Video Out* and *Burst Error* monitor points are mounted on the front panel of the unit.

General Specification

Inputs

Early Video	−2 dB w.r.t. 1 V p-p
Delayed Video	−7 dB w.r.t. 1 V p-p
Syncs (positive-going) (from GE2/504)	1 V p-p
Clamp Correction Signal (from AM3/501)	—
Sync-gating Pulses (from GE2/503)	3·2 V p-p
Burst Error Signal (from AM1/558)	100 mV p-p (approx.)

Input Impedances

Burst Error Signal	variable (about 50 ohms for small error signals, increasing with amplitude)
All Other Inputs	high w.r.t. 75 ohms

Outputs

Clamp Error Signal (to AM3/501)	
Burst-corrected Video	2 dB w.r.t. 1 V p-p
Uncorrected Video (early video)	1 V p-p
Stabilised Video	1 V p-p (when terminated in 75 ohms)

Power Requirements

12 V, 89 mA
+9 V, 70 mA
+4 V, 68 mA
−4 V, 106 mA
14 V, 90 mA

Operating Temperature	0–45°C
Weight	about 1 lb.

Circuit Description

A block diagram of the complete unit is given in Fig. 1. For convenience the circuit diagram is divided into Video Amplifier and Processing Amplifier sections and these are given in Figs. 2 and 3 respectively.

Video Amplifier

The burst-error input signal is applied to a feedback amplifier comprising transistors TR17 and TR18. The signal developed at the emitter of TR18 feeds the *Burst Error* monitor point, the common-base stage TR19 and, via emitter-follower TR20, the negative feedback loop to the base of TR17.

From the collector of TR19 the burst-error signal is applied via buffer emitter-follower TR13 to the junction of R63 and C20, at which point it is added to the video signal. The amplitude of the added signal is determined by the setting of R88; phase correction is provided by C39 and C40.

The video input signal (labelled Early Video in Fig. 2) is applied to a complementary feedback amplifier comprising transistors TR11 and TR12. From this amplifier the signal is applied to a delay network and also to the *Early Video Out* connector.

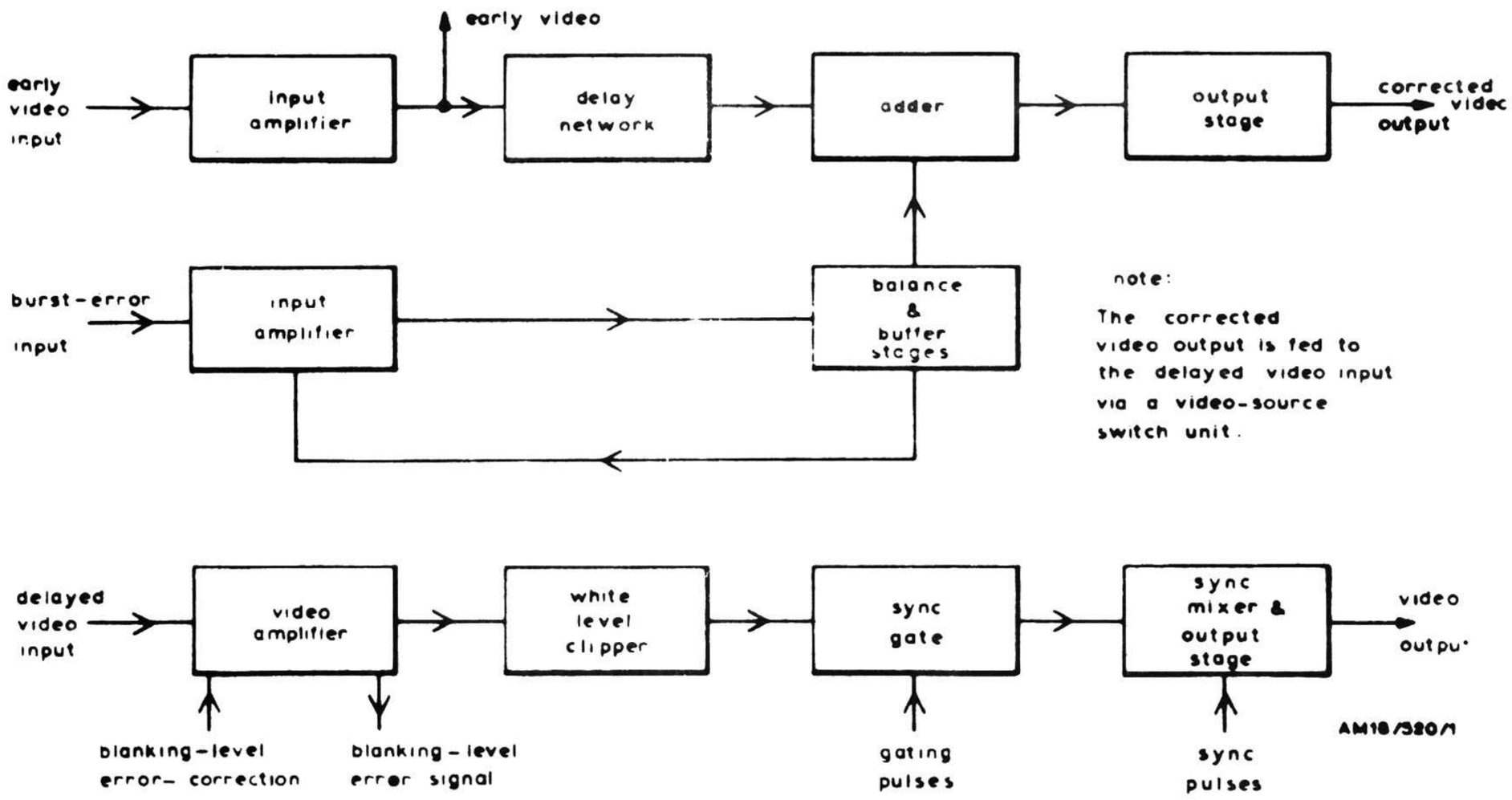


Fig. 1 Block Diagram of the AM18/520

The delay network ensures that the video signal is coincident in time with the burst-error signal when the two signals are combined in the adding stage. The delayed video signal is then added, via emitter-follower TR21, to the burst-error output from TR13 and the error-corrected signal is fed via emitter-coupled pair TR14. TR15 to the output stage TR16

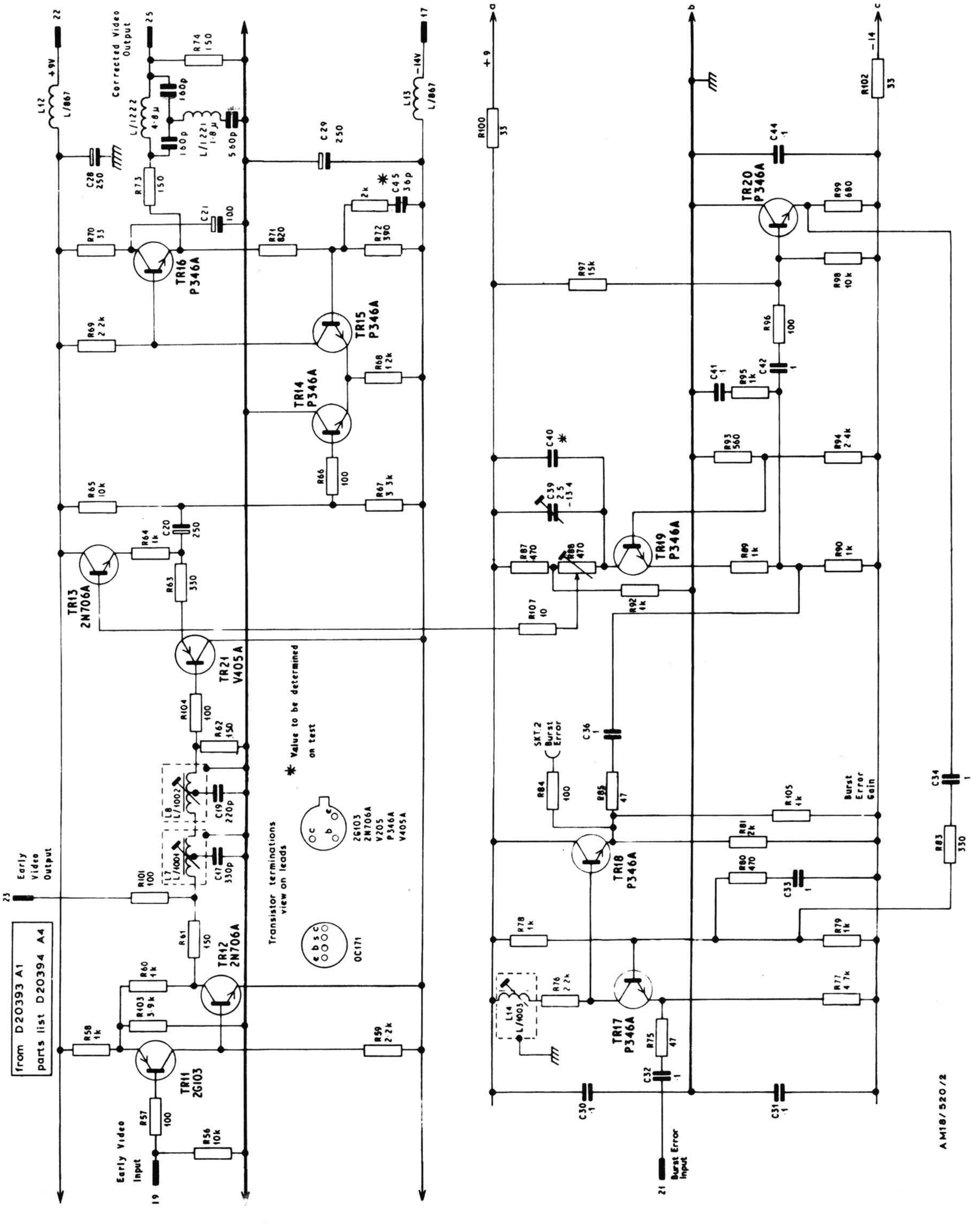
Processing Amplifier

The video input signal is applied via emitter-follower TR1 to emitter-follower TR2. Transistor TR2 is fed also with a blanking-level correction signal derived from the associated Error Signal Amplifier; thus an error-corrected signal is developed at the emitter of TR2. Transistors TR3, TR4 and TR5 form a feedback amplifier; from the emitter of TR5 the signal is fed to the input of the Error Signal Amplifier and to a white-level clipper circuit.

The signal is applied to the clipper diode D1 via a heavily-damped resonant circuit which is tuned to 4·43 MHz; this circuit modifies the action of the clipper and so prevents premature clipping of high-amplitude chrominance information. Variable resistor R17 is a clipping-level control. The clipped signal is then applied, via a potential divider network which reduces the peak-to-peak signal amplitude, to the sync-gating stages. High-frequency correction is provided by capacitors C7 and C8.

The original sync pulses are removed from the signal in two similar diode-resistor bridges which function as gating stages; each stage reduces the sync pulse amplitude by about 26 dB. During the active portion of each line the diodes do not conduct and the signal and the colour-burst pass through the gating stages without attenuation. However, during the sync-pulse periods the diodes are driven into conduction by externally-generated gating pulses[5] and present a low impedance to the signal. Thus the sync pulses are removed by the cumulative action of the two gating stages. Variable resistor R24 is used to control the bias applied to the first gating stage and is adjusted to bring the direct potential at the junction of diodes D2 and D3 to zero volts. Variable resistor R32 performs the same function for the second gating stage. Capacitors C11, C12 and C13 are adjusted on test to reduce to a minimum any spikes caused by the gating process.

The non-composite video output from the second gating stage is applied to emitter-follower TR6. Preset resistor R37 enables the level of the signal applied to the output amplifier to be varied over the range 1 dB. From TR6 the signal is applied to a feedback amplifier comprising transistors TR7 to TR10. Mixed sync pulses[6] are added to the video signal at the base of TR8. Preset resistor R49 is adjusted so that the mean potential at the output terminal is less than 100 millivolts


Corrected Video Output
Early Video Output
Early Video Input
from D20393 A1
parts list D20394 A4
Burst Error Input
SKT.2 Burst Error
Burst Error Gain
Transistor terminations view on leads
2G103 2N706A V205 P346A V405A
OC171
* Value to be determined on test
TR11 2G103
TR12 2N706A
TR13 2N706A
TR14 P346A
TR15 P346A
TR16 P346A
TR17 P346A
TR18 P346A
TR19 P346A
TR20 P346A
TR21 V405A
L12 L/867
L13 L/867
L/1222 4·8µ
L/1221 1·8µ
L7 L/1001
L8 L/1002
L14 L/1003
+9V
−14V
+9
−14
C28 250
C29 250
C20 250
C21 100
C17 330p
C19 220p
C30 1
C31 1
C32 1
C33 1
C34 1
C36 1
C39 2·5 −13·4
C40 *
C41 1
C42 1
C44 1
C45 36p
R57 100
R58 1k
R59 2·2k
R60 1k
R61 150
R62 150
R63 330
R64 1k
R65 10k
R66 100
R67 3·3k
R68 12k
R69 2·2k
R70 33
R71 820
R72 390
R73 150
R74 150
R75 47
R76 2·2k
R77 4·7k
R78 1k
R79 1k
R80 470
R81 2k
R83 330
R84 100
R85 47
R87 470
R88 470
R90 1k
R92 1k
R93 560
R94 2·4k
R95 1k
R96 100
R97 15k
R98 10k
R99 680
R100 33
R101 100
R102 33
R103 3·9k
R104 100
R105 1k
R107 10
AM18/520/2

Alignment

See parent unit[1].

References to Typical Associated Equipment

1. Sync Pulse Stabilising Amplifier AM18/503A.
2. Burst Error Amplifier AM1/558.
3. Video Source Switch Unit UN9/512.
4. Error Signal Amplifier AM3/501.
5. Gating Pulse Generator GE2/503.
6. Pulse Generator GE2/504.

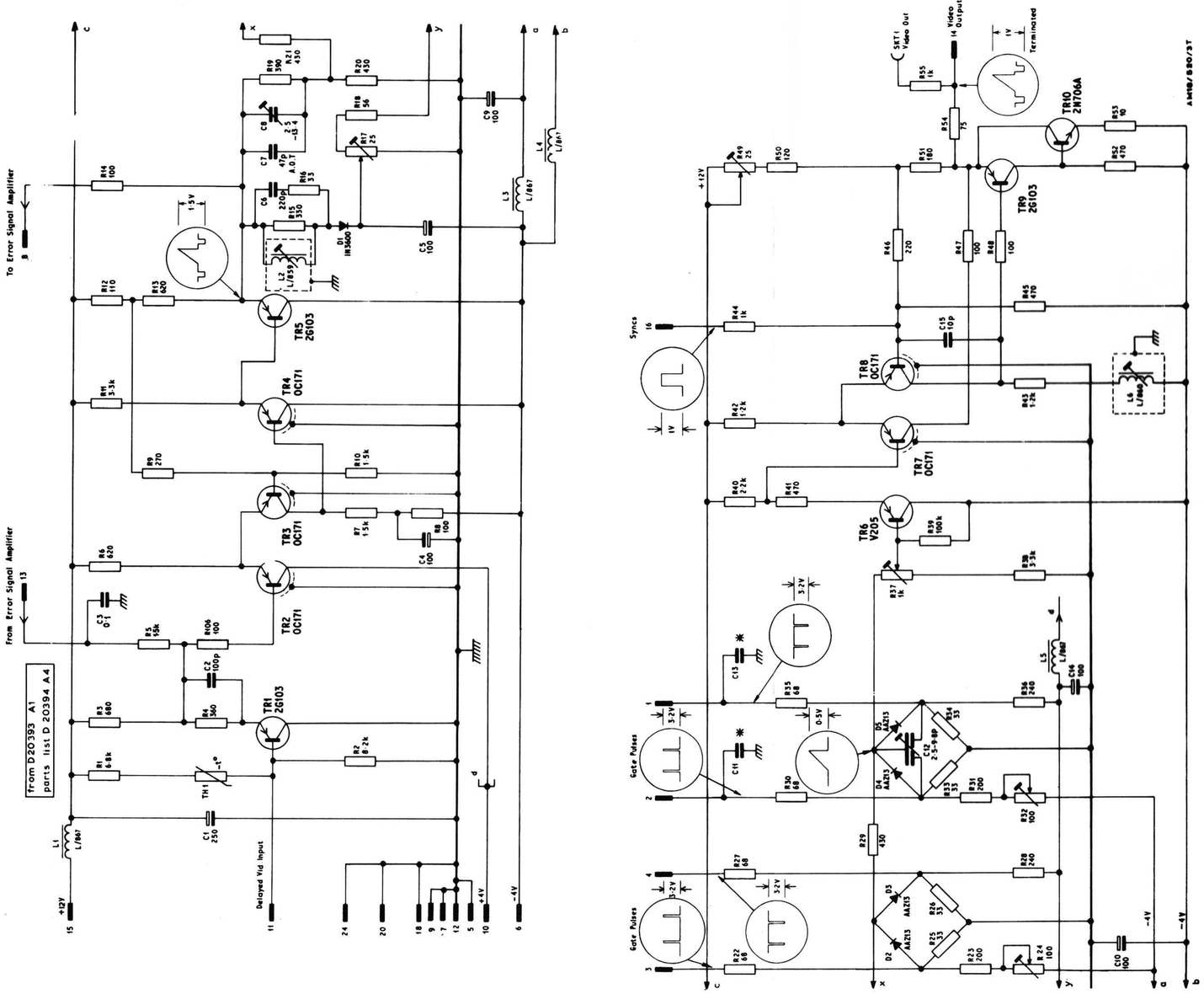
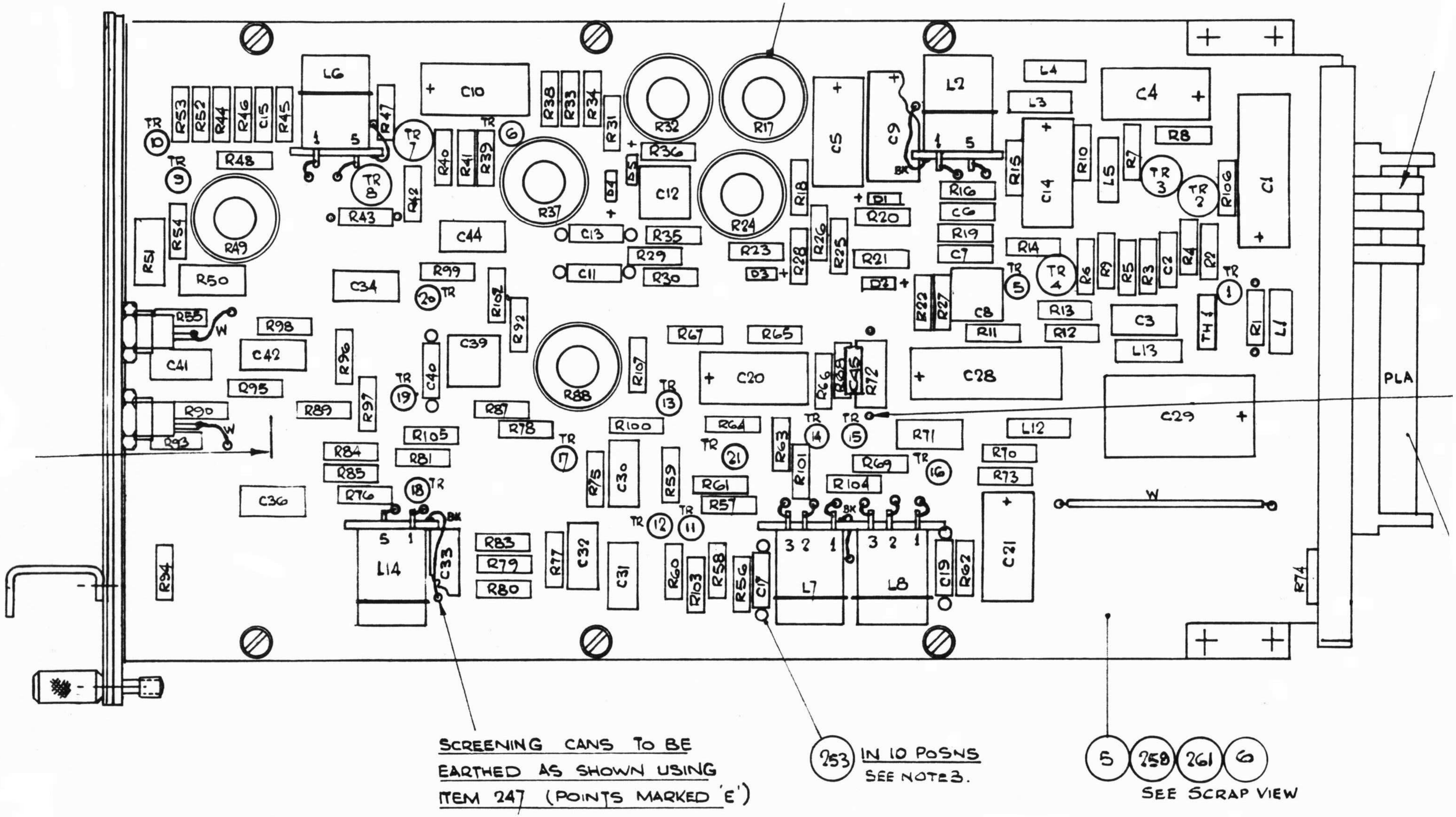


Fig. 3 Circuit of the Processing Amplifier in AM18/520


L6
C10
R53
R52
R44
R46
C15
R45
R47
R48
R49
R51
R54
R50
R43
R42
R40
R41
R39
R38
R33
R34
R31
R32
R17
R36
C12
C13
R35
R29
R30
C11
R37
R24
C5
C9
L2
L4
L3
C4
R8
R15
C14
R10
L5
R7
TR 3
TR 2
R106
C1
R16
C6
R19
C7
R20
R21
R18
R26
R25
R28
R23
R22
R27
C8
R14
TR 4
R6
R9
R5
R3
C2
R4
R2
R13
R12
R11
C3
L13
TH 1
R1
L1
C34
R99
R102
R92
C44
C39
C42
C41
R98
R95
R90
R93
R96
R97
C40
R89
R87
R78
R88
R107
R67
R65
C20
R66
R68
C45
R72
C28
C29
PLA
R105
R84
R85
R76
R81
R100
R64
R63
R101
R71
L12
R70
R73
R69
R104
C36
R94
L14
C33
R83
R79
R80
R77
C32
C31
R75
C30
R59
R61
R57
R60
R103
R58
R56
C17
L7
L8
C19
R62
C21
R74
W
SCREENING CANS TO BE EARTHED AS SHOWN USING ITEM 247 (POINTS MARKED 'E')
253 IN 10 POSNS SEE NOTE 3.
5
250
261
6
SEE SCRAP VIEW

SPAC